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Lithographic Graphitic Memories

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ABSTRACT Reported here are easily accessible memory devices based upon stripes of chemical vapor deposited (CVD) nanosized irregular discs of graphitic material that can be layered in stripes ≤10 nm thick with controllable lengths and widths. These lithographic graphitic stripes, which can be easily fabricated in large quantities in parallel by conventional fabrication techniques (such as CVD and photo- or e-beam lithography), with yields >95%, are shown to exhibit voltage-induced switching behavior, which can be used for two-terminal memories. These memories are stable, rewritable, and nonvolatile with ON/OFF ratios up to 10^7, switching times down to 1 μs (tested limit), and switching voltages down to 3−4 V. The major functional parameters of these lithographic memories are shown to be scalable with the devices' dimensions.

KEYWORDS: graphitic carbon · CVD · nanoscale devices · resistive switching · nonvolatile memories · graphene

Over the past decade, there has grown a demand for truly nanosized electronic switches and memories that can be scaled beyond conventional CMOS counterparts. Numerous nanosized objects, including carbon nanotubes,[1,2] semiconductor nanowires,[3,4] quantum dots,[5] graphene nanoribbons,[6,7] and even individual organic molecules,[8,9] have been proposed and extensively studied as possible candidates for nanoscale electronic devices. However, though some of these recently reported devices exhibit superior performance compared to silicon-based structures, CMOS devices are ultimately unrivaled in terms of fabrication feasibility. While millions of CMOS devices can be made in parallel with high yield by conventional lithographic techniques, fabrication of devices based on individual nanosized objects remains a challenge and often requires state-of-the-art approaches, such as those used to make the electronic devices based on the recently reported graphitic nanocables: dielectric nanowires coated with a thin (~10 nm) layer of carbon,[10] which were shown to exhibit superior two-terminal memory properties.[11] However, graphitic nanocables have the same device fabrication problems that are typical of nanosized objects, such as variation in properties between individual structures and hard-to-achieve placement in specific sites and wiring, and are thus unlikely to become building blocks for large-scale memory arrays. Interestingly, chemical vapor deposited (CVD) amorphous carbon, which has been known for decades, when viewed at the nanoscale domain size, possesses ~5 nm diameter irregular disks of graphitic material that can be arranged in conformal arrays that are 5−10 layers thick. These conformal arrays of CVD graphitic sheets have intriguing properties that could be used for newly emerging applications such as two-terminal memories or programmable vias. The memory-based applications of these CVD-grown graphitic structures are discussed here. The lithographically accessed graphitic memories exhibit voltage-induced two-terminal switching behavior typical of graphitic nanocables,[11] but at the same time, they can be fabricated in large quantities in parallel by conventional techniques with yields >95%. These lithographic graphitic memories are stable, rewritable, and nonvolatile, with up to 10^7 ON/OFF ratios and switching times as short as 1 μs (tested limit). In contrast to nanocables, the major functional parameters of these lithographic memories can be precisely controlled by the fabrication conditions.

Herein we consider two types of conventional lithographically accessible embodiments for the two-terminal graphitic memories: planar (a stripe of CVD-grown carbon bridging two electrodes) and vertical (a CVD carbon film inside the hole connecting top and bottom electrodes). These two embodiments are suitable for various electronic device studies ranging from

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planar reprogrammable interconnects and film-based sensors to densely packed vertical memories and programmable vias. Most of the focus here is upon the planar stripe devices because the graphitic material is easily observed for study, whereas the vertical devices are buried under the top electrode and therefore harder to assess. Nonetheless, the basic vertical device behavior is demonstrated here and shown to be analogous to the planar structure's behavior.

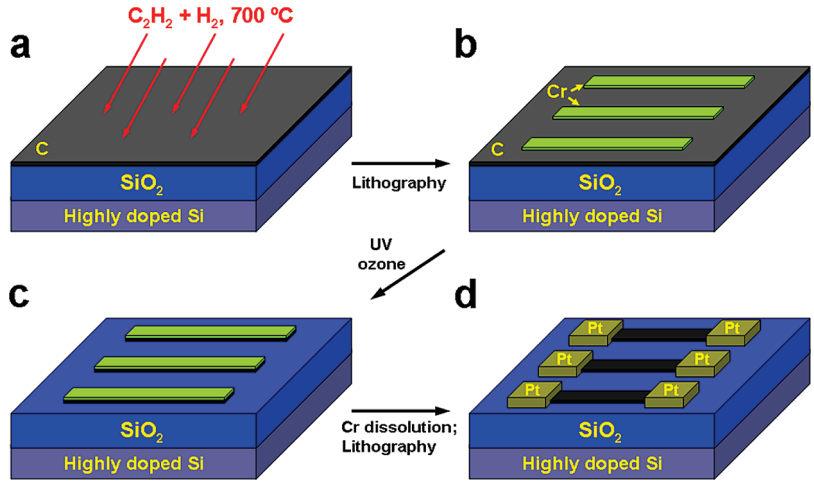

Figure 1. Fabrication of graphitic stripe devices. (a) CVD growth of carbon coatings onto silicon wafers. (b) Photo- or e-beam lithography to fabricate chromium stripes. (c) Removal of unprotected carbon by UV−ozone. (d) Dissolution of chromium and second-step lithography to define platinum contacts atop the stripes to form two-terminal devices.

RESULTS AND DISCUSSION

Two-terminal electronic devices based on graphitic stripes were fabricated according to the general scheme shown in Figure 1 (see Experimental Section for details). We fabricated and tested a series of two-terminal devices with a source−drain length (l) between the electrodes in the range of 0.25−3 μm, a carbon stripe width (w) spanning 0.2−5 μm, and a carbon layer thickness (t) of 5−10 nm. However, we have found that the conductivity of such fabricated devices decreases dramatically with t, so that devices based on 5 nm thick carbon stripes were not as reliably conductive. Therefore, the results of electrical measurements discussed in the following were obtained on the 10 nm thick striped devices.

A top-view scanning electron microscopy (SEM) image of a typical device is shown in Figure 2a. This structure contains 6 two-terminal devices and also provides a testbed for various experiments, such as four-probe electrical measurements and studying the effect of l on the devices' performance. Figure 2b,c shows a typical AFM image of a carbon stripe along with two representative height profiles, suggesting that the synthesized stripes are uniform along their lengths. High-resolution transmission electron microscopy (HRTEM) image of the CVD-grown carbon coating is presented in Figure 2d, in which the amorphous SiO_2 substrate and the carbon layer consisting of discontinuous graphitic sheets are clearly distinguished. It is noteworthy that the graphitic coatings have a layered structure with most of the conformally grown graphitic sheets nearly parallel to the surface of the substrate. These amorphous carbon-derived sheets are about 5 nm in length and extensively buckled. These observations are in agreement with the results of Raman spectroscopy (Figure 2e): spectra of graphitic coatings possess well-pronounced D- and G-bands, indicating the presence of both sp^2 and distorted sp^2 or sp^3 carbon atoms, which is typical for amorphous carbon. According to the results of four-probe electrical measurements, the resistivity of CVD-grown carbon in graphitic stripes is $\sim 4 \times 10^{-3}\ \Omega \cdot \mu m$ (Figure 2f), which is higher than typical values reported for bulk amorphous carbon.[12]

Figure 2f shows that as-fabricated devices exhibited Ohmic behavior at low voltages. However, as the voltage increases, the device exhibits a nonlinear increase in conductance until at some voltage the current drops down with a peak-to-valley ratio >4000 (Figure 3a). We refer to this voltage as the break voltage (V_{break}). SEM images of devices before and after V_{break} clearly demonstrate that the current drops due to the formation of a crack across the carbon stripe (Figure 3b,c). Typically, the width of these cracks varies along its length from ~20 nm to only a few nanometers and occurs near the middle portion of the stripe, a location far from the heat-sinking sites of the electrodes. Similar electrical V_{break} curves were previously reported for different carbon nanomaterials including carbon nanotubes,[13,14] nanowires,[15] and graphene sheets.[16] Interestingly, however, the conductance of the carbon stripes, which had diminished during sweeping the voltage from 0 V to V_{break}, can be restored during the back sweep. Figure 3a shows that the current drastically increases at a voltage of about 10 V upon the back sweep. We will further refer to this characteristic voltage as the switching voltage (V_{switch}) because, after the initial V_{break}, the device will exhibit a transition from a high-conductance state at $V < V_{switch}$ to low-conductance state at $V > V_{switch}$, regardless of the sweep direction. In contrast to the V_{break} of the carbon stripes, the transition from one state to another at around V_{switch} was not associated with observable changes in the corresponding SEM images. Therefore, the changes in the structure at V_{switch} are buried within the crack region, and they are not observable.

The carbon stripe devices possess memory effects because the $I-V$ behavior depends on whether the previous scan was left in a high- or low-conductance state.

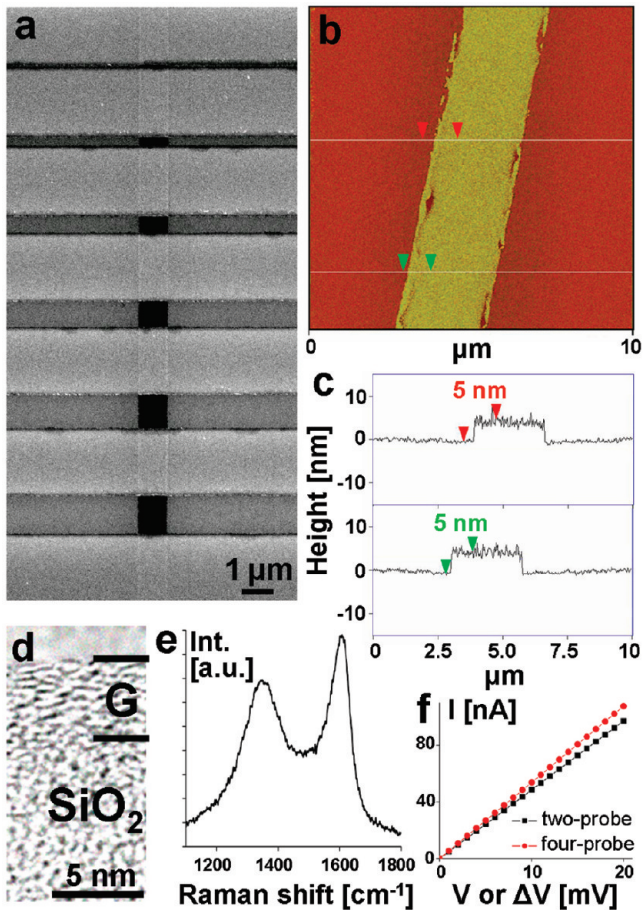

Figure 2. Structural properties of graphitic stripe devices. (a) SEM image of a typical multi-terminal device, where a single 10 nm thick graphitic stripe is contacted by multiple Pt electrodes with varying spacings. (b) AFM image of a typical stripe along with (c) representative height profiles showing that these stripes are 5 nm thick. Note that subsequent electrical data are on 10 nm thick stripes. (d) Fragment of a typical cross-section HRTEM image of graphitic layers (marked as G) on Si/SiO_2 substrate, recorded from a focused ion beam (FIB)-cut surface. The individual graphitic sheets can be seen, and they have a length of ~5 nm each. (e) Raman spectrum of CVD-grown carbon layer on Si/SiO_2 substrate. (f) Electrical properties of a graphitic stripe device (l = 913 nm, w = 2 μm, t = 10 nm) measured by two- and four-probe methods.

This effect is illustrated in Figure 3d by a sequence of $I-V$ curves recorded after V_{break} for the same device, shown in Figure 3a. During the first cyclic voltage sweeping (0 V → 15 V → 0 V), the device is initially in high-conductance state and then transfers to low-conductance state at V_{switch}, and then the conductance is restored at near the same voltage on the back sweep. The subsequent 0 V → 15 V → 0 V scans result in nearly the same $I-V$ curves. However, after a single voltage sweep from 0 to 15 V (Figure 3d, second panel), the $I-V$ behavior of the device changes. During the third bias sweeping under the same conditions, the device starts in a low-conductance state, as it ended in the previous scan, while the high-conduction state is restored at some voltage between 0 and V_{switch}. The following 0 V → 15 V single scans would result in the same $I-V$ behavior with low conductivity at low voltages, until a cyclic voltage sweep (0 V → 15 V → 0 V) is performed (Figure 3d, last panel).

The above results show that two distinct states with low and high conductance at low voltages can be achieved through bias sweep routines. It is noteworthy that, instead of sweeping, voltage pulses can be used to achieve the switching between the ON and OFF states at low bias. The potential working ranges of reading, writing, and erasing are indicated in Figure 3e. The inset in Figure 3e shows that 1 μs (tested limit) 8 V pulses result in a high current of ~20 μA at 1 V, whereas 1 μs 15 V pulses set the device to a low-conductance state with a current of ~10 pA at 1 V. The inset in Figure 3e shows that the data can be read successively 1000 times, using 1 μs 1 V pulses, and these operations do not affect the state of the device. The result shows that no observable degradation occurred after the continuous operation, revealing that the carbon stripe memory is indeed nonvolatile with a nondestructive read and ON/OFF ratio of ~10^6. Furthermore, Figure 3f shows that the same device has been subjected to 1000 "write−10 read−erase−10 read" cycles with no observable change in its performance, attesting to its cyclic endurance. Similar electrical properties were found for more than 200 tested devices (>95% yield) with different source−drain lengths and widths of carbon stripes. We have observed <5% variability in V_{break} between devices with the same dimensions. The variability in V_{switch} was higher, from 10 to 20% for different devices with the same dimensions, which could be attributed to variations in crack formation, especially when viewed at the nanoscale. The ON/OFF ratios recorded for these devices were from 10^4 to 10^7.

Carbon-coated nanocable devices, reported in our previous work to exhibit similar memory behaviors,[11] had difficult-to-predict electrical properties because nanocables, even when grown under the same conditions, had different diameters, non-uniform carbon coating on the curved surfaces, and different contact quality. In contrast, the functional characteristics of graphitic stripe devices, such as V_{break}, V_{switch}, and corresponding currents, can be controlled, within the specifications mentioned above, by defining specific geometrical parameters for the devices. Figure 3g shows several V_{break} $I-V$ curves recorded for devices having different source−drain lengths and carbon stripe widths. For any set of devices with the same w but different l, V_{break} increases with l, whereas the current at V_{break} remains the same, suggesting that l has no effect on the V_{break} current, within the size range measured. In contrast, the width of the stripes has no effect on V_{break}, but affects the maximum current; three current levels w = 0.5, 1, and 2 μm are clearly distinguished in Figure 3g. Though $I-V$ curves for V_{break} on only 11 devices are compared in Figure 3g, the above observations are characteristic for all tested devices.

These results are explainable assuming that the V_{break} of graphitic stripes occurs at a certain

temperature, T_{break}. Then, in order to heat the stripe to T_{break}, V_{break} should be high enough to generate sufficient Joule heat Q, which in the first approximation can be expressed using the basic equation for the specific heat, as in eq 1:

$$Q \propto C \cdot m \cdot T_{break} = C \cdot \rho \cdot l \cdot w \cdot t \cdot T_{break} \quad (1)$$

where C and ρ are the specific heat and density of CVD-grown carbon, respectively. On the other hand, in eq 2 (Joule's law)

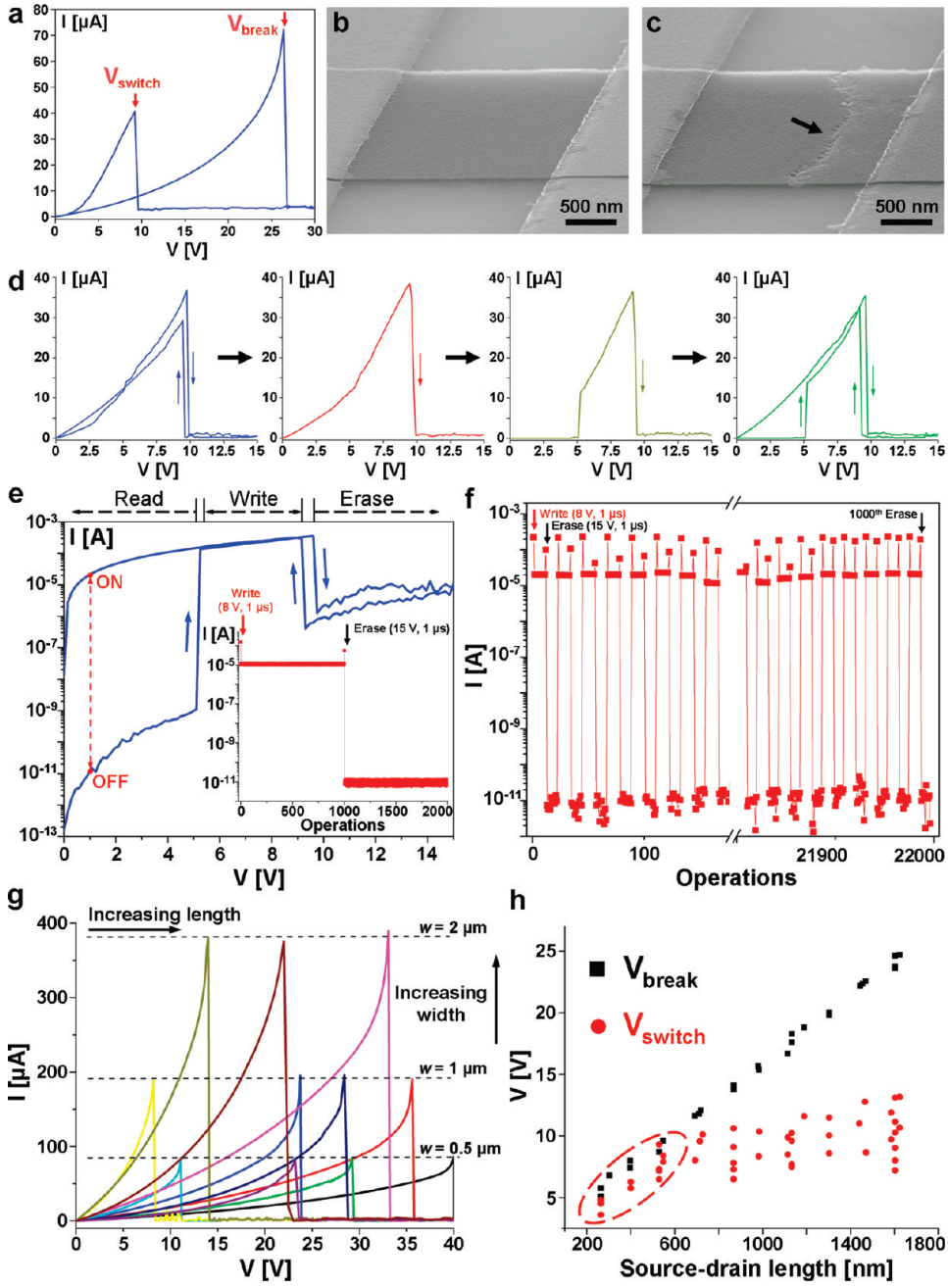

Figure 3. Memory properties of graphitic stripe devices. (a) Electrical break and switching $I-V$ curve recorded for a device with $l = 1.8$ μm, $w = 2$ μm, and $t = 10$ nm. (b,c) Tilted-view SEM images of two different devices before and after V_{break}, respectively. The arrow shows the crack across the stripe formed due to V_{break}. (d) Sequence of $I-V$ curves recorded after V_{break} for the same device, shown in (a); see text for details. (e) Logarithmic $I-V$ characteristics of the same device; the high- and low-conductance states of the device can be achieved through voltage pulses in the "Write" and "Erase" regions, respectively. After writing or erasing, the state of the system is recorded in the "Read" voltage region. The inset shows memory performance of the same device; pulses of +8 V for 1 μs turn the device to the ON state, and +15 V pulses for 1 μs change the device to the OFF state. After each write/erase operation, the device current was consecutively read at +1 V 1000 times. (f) Cyclic endurance of the same device: pulses of +8 and +15 V for 1 μs were used for writing and erasing, respectively. After each write/erase operation, the device current was consecutively read at +1 V 10 times. After 1000 cycles of write−read (10×) − erase−read (10×) operations, the memory showed no degradation of its ON−OFF current readings. (g) $I-V$ curves for V_{break} for devices with different dimensions. (h) Dependences of V_{break} and V_{switch} on the source−drain length (l) for the set of devices with $w = 1$ μm and $t = 10$ nm. The dashed oval shows a region where V_{break} and V_{switch} are comparable.

$$Q = \frac{V_{break}^2}{R}\tau = \frac{V_{break}^2 \cdot w \cdot t \cdot \tau}{\gamma \cdot l} \quad (2)$$

the Joule heat is related to the time (τ) and resistivity (γ) of CVD-grown carbon, respectively. Combining eqs 1 and 2, we obtain eq 3:

$$V_{break} \propto \sqrt{\frac{C \cdot \rho \cdot \gamma \cdot T_{break}}{\tau}} \cdot l = A \cdot l \quad (3)$$

where A is independent of geometric parameters of the devices. Thus, V_{break} linearly depends on the l and is independent of w and t, which is in agreement with our observations. Similarly, the current at V_{break} is independent of l and linearly depends on w and t, which also agrees with the experimental results.

The dependences of V_{break} and V_{switch} on l for the set of devices with $w = 1$ μm, $t = 10$ nm, and different values of l are shown in Figure 3h. Apparently, V_{break} linearly depends on l, as shown above, whereas V_{switch} also decreases with l. Interestingly, when we were studying similar switching phenomena in graphitic nanocables,[11] we could not distinguish the V_{break} as an individual stage because the V_{break} and the subsequent V_{switch} were nearly the same. Figure 3h also suggests that, as l decreases below ~ 600 nm, V_{break} and V_{switch} become comparable in magnitude. Though the exact relationship between V_{switch} and l is difficult to derive, the linear dependence of V_{break} on l could serve as an upper approximation since $V_{switch} \leq V_{break}$. For the shortest devices fabricated in this work ($l = 250$ nm), V_{break} and V_{switch} could be as low as 3−4 V. We expect that for smaller devices these voltages should be even lower, an important consideration for large-array memory applications.

Essential for dense memory arrays and programmable vias is the need for similar switching in vertical graphitic devices. The schematic of the fabrication procedure for these devices is shown in Figure 4a (see Experimental Section for details); SEM images in Figure 4a demonstrate the appearance of a typical hole after the fabrication steps.

The vertical devices were tested under vacuum using a W probe to touch the highly doped silicon substrate and another micrometer-manipulated W probe to touch the platinum top electrodes. Typical results are shown in Figure 4b,c, revealing the resistive switching behavior and memory effects similar to those observed for the planar graphitic devices. Though it is difficult to directly study the physical properties of carbon buried under the Pt top contact, the similarities between the planar and vertical devices suggest that the resistive switching in the latter is also associated with cracking of the carbon deposit inside the hole. Interestingly, the results of SEM analyses of the cut devices (exposed by chip cleavage) suggest that some holes may have relatively large voids due to conformal growth and closure of the top before complete carbon-filling occurs. In these cases, the crack would form in the thinnest part, as shown schematically in the inset in Figure 4b.

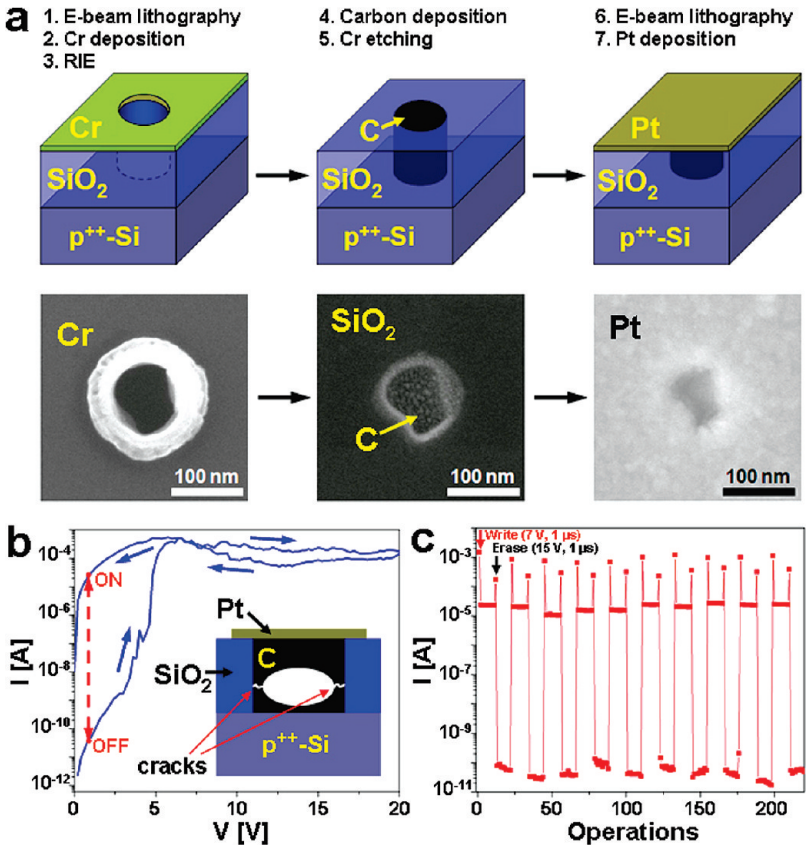

Figure 4. Fabrication and electrical properties of the vertical graphitic devices. (a) Process flow for obtaining carbon films within oxide holes that ultimately have a Si bottom contact and a Pt top contact (see text for details) is shown at the top, while the corresponding SEM images at each step are shown below. (b) $I-V$ behavior while the inset shows the presumed crack within the filled or partially carbon-filled (as shown) hole that is generated upon voltage sweeping. (c) Cyclic memory operations of the vertical device writing at 7 V and erasing at 15 V for 1 μs each.

Similar transitions from states with different conductance have recently been reported for other carbon-based devices.[11,16−18] Interestingly, in all of those studies, the resistive switching was proposed to be filamentary in nature. In our case, the filaments could form at some voltage close to V_{switch}, bridging the crack produced at V_{break}, and then rupture at $V > V_{switch}$. However, the exact origin of the filament remains unclear. For instance, similar switching in graphene devices was attributed to the formation and breaking of carbon atomic chains that bridge junctions.[16] Another recent work on resistive switching in devices based on carbon nanotubes and diamond-like carbon suggests that the filaments are made of conductive sp^2 carbon inclusions within a nonconductive

sp^3 carbon matrix.[17] Similar resistive switching has been recently reported for a carbon-based nanogap junction composed of single-wall carbon nanotubes with encapsulated fullerenes; the authors propose that the migration of fullerene molecules causes the filament formation.[18] Upon the basis of our HRTEM observations, we have proposed that individual 5 nm graphitic sheets, which constitute the CVD-grown carbon coatings, could serve as filaments to bridge the gap; in these cases, the switching mechanism could also be interpreted as nanoelectromechanical in nature,[11] although any further precision in assignment is difficult to define. Recent studies also suggest that the SiO_2 substrate underneath voltage-induced heated material can be severely damaged by the high temperature or electric field;[19] this might play a role in the switching mechanism in the graphitic devices described here.

Though a better understanding of the mechanism would be helpful, what are presently apparent are the unique memory properties of the planar and vertical graphitic devices. The stability, resilience, nonvolatility, ON/OFF ratios up to 10^7, switching times to the tested 1 μs, and switching voltages down to 3−4 V, combined with predictable, fabrication-controlled $I-V$ behavior, simple two-terminal geometry, and access to mass fabrication by CVD and photolithography with yields >95%, make them attractive structures for memories and possible other device applications.

EXPERIMENTAL SECTION

Fabrication of Planar Graphitic Devices. Figure 1 shows the schematic of the fabrication process. In the first step, a thin carbon layer was deposited onto Si/SiO_2 substrates using a CVD process (Figure 1a), namely, thermal decomposition of acetylene diluted by hydrogen ($V(C_2H_2):V(H_2) = 1:3$) at 700 °C in a tube furnace. The synthesis conditions were adjusted to achieve an average carbon layer growth rate of 1 nm/min. Si/SiO_2 substrates covered by carbon films with thicknesses ranging from 5 to 10 nm were fabricated, as determined by AFM. In the second step, arrays of 50 nm thick chromium stripes were fabricated by standard photo- or e-beam lithography (Figure 1b). Then, the substrates were subjected to UV−ozone to remove carbon everywhere except underneath the Cr stripes (Figure 1c). Finally, Cr was removed by CR-7 chromium etchant solution (Cyantek), and the formed graphitic stripes were contacted by Pt pads made by a second lithography step (Figure 1d).

Fabrication of Vertical Graphitic Devices. The schematic of the fabrication procedure is shown in Figure 4a. First, individual 50 nm thick Cr pads, each containing a sub-100 nm hole, were made by the standard e-beam lithography on top of a heavily doped p-type silicon wafer with a 200 nm thick thermal SiO_2 layer. Then, silicon oxide was etched through the above holes all the way down to p^{++}-Si by reactive ion etching (RIE, CF_4). The obtained holes were carbon-filled as described above. After the holes were inspected by SEM and found to appear filled, the excess carbon around the holes was removed by ultrasonication-assisted etching of the Cr pads with a CR-7 chromium etchant solution. In the final step, the Pt top contact was fabricated atop each hole by the second step e-beam lithography.

Device Characterization. SEM imaging was performed on a JEOL-6500 field-emission microscope. AFM images were obtained with a Digital Instruments Nanoscope IIIa, operating in tapping mode, using Si tips n-doped with 1−10 Ω · cm phosphorus (Veeco, MPP-11100-140) at a scan rate of 0.5 Hz and a resolution of 512 × 512. Raman spectroscopy was performed on a Renishaw Raman microscope using a 633 nm HeNe laser. TEM imaging was performed on a JEOL-2100F microscope. The electrical properties of devices were tested using a probe station (Desert Cryogenics TT-probe 6 system) under vacuum with chamber base pressure below 1×10^{-5} mm Hg. The $I-V$ data were collected by an Agilent 4155C semiconductor parameter analyzer, while some of the pulse measurements were performed with a National Instruments USB-6259 multifunction data acquisition module.

REFERENCES AND NOTES

1. Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic Circuits with Carbon Nanotube Transistors. *Science* **2001**, *294*, 1317–1320.
2. Rueckes, T.; Kim, K.; Joselevich, E.; Tseng, G. Y.; Cheung, C. L.; Lieber, C. M. Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing. *Science* **2000**, *289*, 94–97.
3. Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L. J.; Kim, K. H.; Lieber, C. M. Logic Gates and Computation from Assembled Nanowire Building Blocks. *Science* **2001**, *294*, 1313–1316.
4. Lu, W.; Lieber, C. M. Semiconductor Nanowires. *J. Phys. D: Appl. Phys.* **2006**, *39*, R387–R406.
5. Klein, D. L.; Roth, R.; Lim, A. K. L.; Alivisatos, A. P.; McEuen, P. L. A. Single-Electron Transistor Made from a Cadmium Selenide Nanocrystal. *Nature* **1997**, *389*, 699–701.
6. Wang, X.; Ouyang, Y.; Li, X.; Wang, H.; Guo, J.; Dai, H. Room-Temperature All-Semiconducting Sub-10-nm Graphene Nanoribbon Field-Effect Transistors. *Phys. Rev. Lett.* **2008**, *100*, 206803.
7. Kosynkin, D. V.; Higginbotham, A. L.; Sinitskii, A.; Lomeda, J. R.; Dimiev, A.; Price, B. K.; Tour, J. M. Longitudinal Unzipping of Carbon Nanotubes to Form Graphene Nanoribbons. *Nature* **2009**, *458*, 872–876.
8. Chen, J.; Reed, M. A.; Rawlett, A. M.; Tour, J. M. Large On−Off Ratios and Negative Differential Resistance in a Molecular Electronic Device. *Science* **1999**, *286*, 1550–1552.
9. Blum, A. S.; Kushmerick, J. G.; Long, D. P.; Patterson, C. H.; Yang, J. C.; Henderson, J. C.; Yao, Y.; Tour, J. M.; Shashidhar, R.; Ratna, B. R. Molecularly Inherent Voltage-Controlled Conductance Switching. *Nat. Mater.* **2005**, *4*, 167–172.
10. Li, Y. B.; Bando, Y.; Golberg, D. SiC−SiO_2−C Coaxial Nanocables and Chains of Carbon Nanotube−SiC Heterojunctions. *Adv. Mater.* **2004**, *16*, 93–96.
11. Li, Y.; Sinitskii, A.; Tour, J. M. Electronic Two-Terminal Bistable Graphitic Memories. *Nat. Mater.* **2008**, *7*, 966–971.
12. Lide, D. R., Ed. *CRC Handbook of Chemistry and Physics*; CRC Press: Boca Raton, FL, 1995−1996; Vol. 76.
13. Collins, P. G.; Hersam, M.; Arnold, M.; Martel, R.; Avouris, R. Current Saturation and Electrical Breakdown in Multiwalled Carbon Nanotubes. *Phys. Rev. Lett.* **2001**, *86*, 3128–3131.
14. Deshpande, V. V.; Chiu, H. Y.; Postma, H. W. C.; Miko, C.; Forro, L.; Bockrath, M. Carbon Nanotube Linear Bearing Nanoswitches. *Nano Lett.* **2006**, *6*, 1092–1095.
15. Jin, C. H.; Wang, J. Y.; Chen, Q.; Peng, L. M. *In Situ* Fabrication and Graphitization of Amorphous Carbon Nanowires and Their Electrical Properties. *J. Phys. Chem. B* **2006**, *110*, 5423–5428.
16. Standley, B.; Bao, W.; Zhang, H.; Bruck, J.; Lau, C. N.; Bockrath, M. Graphene-Based Atomic-Scale Switches. *Nano Lett.* **2008**, *8*, 3345–3349.
17. Kreupl, F.; Bruchhaus, R.; Majewski, P.; Philipp, J. B.; Symanczyk, R.; Happ, T.; Arndt, C.; Vogt, M.; Zimmermann,

R.; Buerke, A.; Graham, A. P.; Kund, M. Carbon-Based Resistive Memory. *Proc. IEEE Electron Devices Meeting* **2008**, 521–524.
18. Naitoh, Y.; Yanagi, K.; Suga, H.; Horikawa, M.; Tanaka, T.; Kataura, H.; Shimizu, T. Non-Volatile Resistance Switching Using Single-Wall Carbon Nanotube Encapsulating Fullerene Molecules. *Appl. Phys. Express* **2009**, *2*, 035008.
19. Yao, J.; Zhong, L.; Zhang, Z.; He, T.; Jin, Z.; Wheeler, P. J.; Natelson, D.; Tour, J. M. Resistive Switching in Nanogap Systems on SiO_2 Substrates. *Small*, in press.